IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
REQUEST FOR FILING NATIONAL PATENT APPLICATION
Under 35 USC 111(a) and Rule 53(b)

PATENT APPLICATION

Asst. Commissioner of Patents
Washington, D.C. 20231

WITH SIGNED DECLARATION

NONPROVISIONAL
NON REISSUE
NON PCT NAT PHASE

jc685 U.S. PTO

09/15/00

jc893 U.S. PTO
09/663340
09/15/00

Sir:

Herewith is the PATENT APPLICATION of
Inventor(s): HAMADA

Title POWER SEMICONDUCTOR DEVICE AND PRODUCTION METHOD FOR THE SAME

Atty. Dkt.: PM 271420 (M#) | TFN990143-US (Client Ref)

including:

Date: September 15, 2000

1. Specification: 14 pages (only spec. and claims) 2. ☐ Specification in non-English language
3. Declaration ☒ Original ☐ Facsimile/Copy ☒ Abstract 1 page(s); 18 numbered claims
4. ☒ Drawings: 3 sheet(s) ☐ informal; ☒ formal of size: ☒ A4 ☐ 11"
5. ☐ See top first page re prior Provisional, National or International application(s). ("X" box only if info is there and do not complete corresponding item 5 or 6). (Prior M# ______ SN ______)
6. **AMEND the specification** please by inserting before the first line: -- This is a ☐ Continuation-in-Part ☐ Divisional ☐ Continuation ☐ Substitute Application (MPEP 201.09) of:

6(a) ☐ National Appln. No. ____/____ filed ______. (M# ____)

6(b) ☐ International Appln. No. ______ filed ______

______ .--

7. ☐ **AMEND the specification** by inserting before the first line: -- This application claims the benefit of U.S. Provisional Application No. 60/ ______, filed ______ . --
8. ☒ Attached is an assignment and cover sheet. Please return the recorded assignment to the undersigned.
9. ☐ Prior application is assigned to ______

   by Assignment recorded ______ Reel ______ Frame ______

10. **FOREIGN** priority is claimed under 35 USC 119(a)-(d)/365(b) based on filing in Japan (country)
11.

Application No.	Filing Date	Application No.	Filing Date
(1) 11-262861	September 17, 1999	(2)	
(3)		(4)	
(5)		(6)	
(7)		(8)	
(9)		(10)	

12. 1 (No.) Certified copy (copies): ☒ attached; ☐ previously filed (date) ______
    in U.S. Application No. ____/____ filed on ______

13. ☐ Attached: ________ (No.) Verified Statement(s) establishing "small entity" status under Rules 9 & 27.

14. **DOMESTIC/INTERNATIONAL** priority is claimed under 35 USC 119(e)/120/365(c) based on the following provisional, nonprovisional and/or PCT international application(s):

Application No.	Filing Date	Application No.	Filing Date
(1)		(4)	
(2)		(5)	
(3)		(6)	

15. ☐ This application is being filed under Rule 53(b)(2) since an inventor is named in the enclosed Declaration who was not named in the prior application.

16. ☒ Attached: Form PTO-1449 listing the enclosed documents

17. ☐ Preliminary Amendment:

THE FOLLOWING FILING FEE IS BASED ON CLAIMS AS FILED LESS ANY ABOVE CANCELLED

				Large/Small Entity		Fee Code
18. Basic Filing Fee				$690/$345	$690	101/201
19. Total Effective Claims	18	minus 20 =	*0	x $18/$9 =	+ 0	103/203
20. Independent Claims	2	minus 3 =	*0	x $78/$39 =	+ 0	102/202
				*If answer is zero or less, enter "0"		
21. If any proper multiple dependent claim (ignore improper) is present , add (Leave this line blank if this is a reissue application)				+ $260/$130	+ 0	104/204
22.				TOTAL FILING FEE ENCLOSED =	$690	
23. If "non-English" box 2 is X'd, add Rule 17(k) processing fee				+ $130	+ 0	139
24. If "assignment" box 8 is X'd, add recording fee				+ $40	+ 40	581
25. ☐ Attached is a Petition/Fee under Rule No.				+ $130	+ 0	122
26.				TOTAL FEE ENCLOSED =	$730	

Our Deposit Account No. 03-3975

Our Order No. 20847 | 271420

C# | M#

CHARGE STATEMENT: The Commissioner is hereby authorized to charge any fee specifically authorized hereafter, or any missing or insufficient fee(s) filed, or asserted to be filed, or which should have been filed herewith or concerning any paper filed hereafter, and which may be required under Rules 16-18 (missing or insufficient fee only) now or hereafter relative to this application and the resulting Official document under Rule 20, or credit any overpayment, to our Account/Order Nos. shown above for which purpose a duplicate copy of this sheet is attached.

This CHARGE STATEMENT does not authorize charge of the issue fee until/unless an issue fee transmittal form is filed.

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APPLICATION UNDER UNITED STATES PATENT LAWS

Atty. Dkt. No. PM 271420
(M#)

Invention: POWER SEMICONDUCTOR DEVICE AND PRODUCTION METHOD FOR THE SAME

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This is a:

- ☐ Provisional Application
- ☒ Regular Utility Application
- ☐ Continuing Application
  - ☒ The contents of the parent are incorporated by reference
- ☐ PCT National Phase Application
- ☐ Design Application
- ☐ Reissue Application
- ☐ Plant Application
- ☐ Substitute Specification
  Sub. Spec Filed ______
  in App. No. ___/___
- ☐ Marked up Specification re
  Sub. Spec. filed ______
  In App. No ___/___

SPECIFICATION

POWER SEMICONDUCTOR DEVICE AND PRODUCTION METHOD FOR THE SAME

INCORPORATION BY REFERENCE

The disclosure of Japanese Patent Application No. HEI 11-262861 filed on September 17, 1999 including the specification, drawings and abstract is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a power semiconductor device and a production method for the power semiconductor device and, more particularly, to a power semiconductor device having a plurality of linear trench gates that extend substantially parallel to one another and extend through a body region formed on a semiconductor substrate, from an obverse surface side of the body region.

2. Description of the Related Art

As a power semiconductor device, an insulated gate bipolar transistor (IGBT) in which N-type emitters formed in contact with trench gates are connected by N-type semiconductor regions so as to form a ladder-like configuration has been proposed (e.g., in Japanese Patent Application Laid-Open No. HEI 9-270512). In this device, the emitter-contact width is reduced by forming ladder-like N-type semiconductor regions. In this device, the N-type

emitters and the N-type semiconductor regions are formed by a single diffusion layer, and therefore, their depths are substantially equal.

In power semiconductor devices, both low on-resistance and high breakdown ruggedness are demanded.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the invention to provide a power semiconductor device with low on-resistance and high breakdown ruggedness.

An insulated gate type semiconductor device according to the invention includes a body region of a first conductivity type formed in a semiconductor substrate, a plurality of trench gates extending through the body region, and a plurality of first semiconductor regions of a second conductivity type that is different from the first conductivity type. The first semiconductor regions have a first depth as measured from a surface of the body region and sandwich the trench gates via the gate-insulating films. The semiconductor device also includes a plurality of second semiconductor regions of the second conductivity type having a second depth as measured from the surface of the body region that is less than the first depth. The second semiconductor regions connect the plurality of first semiconductor regions spaced apart from one another.

According to the above-described aspect, since the second semiconductor regions are formed to have less depth than the first semiconductor regions, the impurity

concentration in a portion of the body region near the second semiconductor region can be increased, in comparison with a case where the first and second semiconductor regions have substantially equal depths. Therefore, the resistance in the portion of the body region near the second semiconductor region is decreased, so that the on-resistance of the semiconductor device can be reduced and the breakdown ruggedness thereof can be improved.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and further objects, features and advantages of the invention will become apparent from the following description of a preferred embodiment with reference to the accompanying drawings, wherein like numerals are used to represent like elements and wherein:

FIGURE 1 is a schematic illustration of a power semiconductor device according to an embodiment of the invention;

FIGURE 2 is a schematic plan view illustrating a construction of the power semiconductor device of the invention;

FIGURE 3 is a graph indicating relationships between depths of a body, a trench-emitter region and an emitter-connecting region from their surfaces and impurity concentrations;

FIGURE 4A illustrates the flow of current occurring where an emitter-connecting region is relatively shallow; and

FIGURE 4B illustrates the flow of current occurring where an emitter-connecting region is relatively deep.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

A preferred embodiment of the invention will be described hereinafter with reference to the accompanying drawings.

FIGURE 1 is a schematic diagram illustrating a construction of a power semiconductor device 20 according to an embodiment of the invention. FIGURE 2 is a schematic illustration of a construction of the power semiconductor device 20 viewed from a surface thereof. A construction on section A-A indicated in FIGURE 2 corresponds to a leftward front face of the illustration of FIGURE 1 (see an arrow A in FIGURE 1). A construction taken on section B-B indicated in FIGURE 2 corresponds to a rightward front face of the illustration of FIGURE 1 (see an arrow B in FIGURE 1). A construction taken on section C-C indicated in FIGURE 2 corresponds to a right side face of the illustration of FIGURE 1 (see an arrow C in FIGURE 1).

The power semiconductor device 20 of this embodiment, as shown in the drawings, has a body 24 of a P^--type semiconductor region formed on a surface of an N^--type epitaxial layer 22 that is formed on a substrate 21 formed by a P-type or N-type semiconductor. A plurality of trench gates 26 are disposed parallel to one another and extend from an obverse surface, which in FIGURE 1 is the top surface, of a semiconductor substrate through the body 24

to the epitaxial layer 22. Formed on opposite sides of each trench gate 26 are emitter regions that are N^+-type semiconductor regions contacting the trench gate 26 via a gate-insulating film 27, such as a silicon oxide film or the like. In this embodiment, the emitter regions are formed by trench-emitter regions 28 (a first semiconductor region) and emitter-connecting regions 30 (a second semiconductor region). The emitter-connecting regions 30 connect trench-emitter regions 28 that face each other so as to form a ladder-like configuration. The power semiconductor device 20 further has contact P regions 32 that are P^+-type semiconductor regions formed between the emitter-connecting regions 30 on the body 24. The power semiconductor device 20 may be a power MOSFET (where the substrate 21 is of N-type), an insulated gate bipolar transistor (IGBT, where the substrate 21 is of P-type) which is a generally-termed vertical-type device wherein a main current flows in a vertical direction with respect to the substrate, or a composite device that partially has a construction of a device mentioned above. FIGURES 1 and 2 show design pattern for the power semiconductor device 20. The contact P region 32 and the trench-emitter regions 28 can be formed by thermal diffusion. Therefore, in a practical manner, a part of the contact P region 32 and a part of the trench-emitter regions 28 may overlap each other.

As shown in FIGURE 1, each trench gate 26 is formed

so as to extend from the obverse surface into the interior of the semiconductor substrate, that is, so as to form an indentation. Furthermore, as shown in FIGURE 2, the trench gates 26 are connected at end portions thereof to a gate voltage-applying circuit conductor 36 (see an upper portion of FIGURE 2). Upper ends of the trench gate 26 are preferably flush with the obverse surface of the semiconductor substrate. In many actual cases, however, the ends of the trench gates 26 are disposed several tenths of 1 μm below the obverse surface of the semiconductor substrate in order to achieve process consistency. Considering this, this embodiment has a construction wherein the upper ends of the trench gates 26 are lower than the obverse surface of the semiconductor substrate.

The N^+ trench-emitter regions 28 are formed deeper than the upper ends of the trench gates 26 so that a portion of each N^+ trench-emitter region 28 contacts the trench gate 26 via the gate-insulating film 27, such as a silicon oxide film or the like. For example, if the upper ends of the trench gates 26 are several tenths of 1 μm lower than the obverse surface of the semiconductor substrate, it is preferable that the N^+ trench-emitter regions 28 be formed to have a depth of about 1 μm.

The N^+ emitter-connecting regions 30 are formed to have a less depth than the N^+ trench-emitter regions 28. As shown in FIGURE 2, a portion of the surface of each N^+ emitter-connecting region 30 is covered, together with a

surface of the adjacent contact P region 32, with a circuit conductor 38. The N^+ emitter-connecting regions 30 are formed in order to electrically connect the N^+ trench-emitter regions 28 and the circuit conductors 38. Therefore, it is required that the N^+ emitter-connecting regions 30 have a low resistance value and such an impurity concentration that the contact resistance with respect to the circuit conductors 38 can be sufficiently reduced.

Characteristics of the above-described power semiconductor device 20 of the embodiment will be described. FIGURE 3 is a graph indicating relationships between depths of the body 24, the N^+ trench-emitter regions 28 and the N^+ emitter-connecting regions 30 measured from their surfaces and impurity concentrations therein. Typically, the body 24, the N^+ trench-emitter regions 28 and the N^+ emitter-connecting regions 30 are formed by thermal diffusion of impurities from the obverse surface side of the semiconductor substrate. Therefore, with increases in the depth from the surface of the semiconductor substrate, the impurity concentration decreases (the diffusion becomes more difficult). That is, the deeper the N^+ emitter-connecting regions 30, the lower the impurity concentration in portions of the body 24 near lower portions of the N^+ emitter-connecting regions 30. The resistance of the body 24 increases with decreases in the impurity concentration therein. Therefore, the resistance of portions of the body 24 near lower portions of the N^+ emitter-connecting regions

30 increases as the depth of the N^+ emitter-connecting regions 30 is increased. FIGURES 4A and 4B exemplify the flow of current occurring if the N^+ emitter-connecting regions 30 are relatively shallow, and the flow of current occurring if the N^+ emitter-connecting regions 30 are relatively deep. In FIGURES 4A and 4B, portions indicated by broken lines represent parasitic NPN transistors present in the devices. Now considered will be a case where current flows from the epitaxial layer 22 through a vicinity of a lower portion of an N^+ emitter-connecting region 30 into a contact P region 32 as indicated by an arrow in each diagram. The resistance of the vicinity of the lower portion of the N^+ emitter-connecting region 30 increases as the depth of the N^+ emitter-connecting region 30 is increased. Therefore, the electric potential that occurs in the vicinity of the lower portion of the N^+ emitter-connecting region 30 also increases when the depth of the N^+ emitter-connecting region 30 is increased. If such an electric potential occurs, it may happen that a forward bias is applied to the base of the parasitic NPN transistor (that is, the parasitic NPN transistor operates) so that the power semiconductor device 20 breaks. In contrast, if the N^+ emitter-connecting region 30 is relatively shallow, the resistance of the vicinity of the lower portion of the N^+ emitter-connecting region 30 is reduced so as to substantially avoid the aforementioned operation of the parasitic NPN transistor. Therefore,

avalanche breakdown ruggedness and latch-up ruggedness (that is, the level of withstanding excessive current) are improved.

In the above-described power semiconductor device 20 of the embodiment, by reducing the depth of the N^+ emitter regions 30, the avalanche ruggedness and the latch-up ruggedness can be improved with controlling the on-resistance.

Although in the power semiconductor device 20 of the embodiment, the body 24 is formed as a P-type semiconductor region, it is also possible to form the body 24 as an N-type semiconductor region and form the epitaxial layer 22, the N^+ trench-emitter regions 28, the N^+ emitter-connecting regions 30 and the P^+ contact region 32 by semiconductor regions of different conduction types.

While the invention has been described with reference to what is presently considered to be a preferred embodiment thereof, it is to be understood that the invention is not limited to the disclosed embodiment or constructions. On the contrary, the invention is intended to cover various modifications and equivalent arrangements without departing from the gist of the invention.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a body region of a first conductivity type formed in a semiconductor substrate;

a plurality of trench gates extending through the body region;

a plurality of first semiconductor regions of a second conductivity type that is different from the first conductivity type, the first semiconductor regions having a first depth as measured from a surface of the body region and sandwiching the trench gates via the gate-insulating films; and

a plurality of second semiconductor regions of the second conductivity type having a second depth as measured from the surface of the body region that is less than the first depth,

wherein the second semiconductor regions connect the plurality of first semiconductor regions spaced apart from one another.

2. A semiconductor device according to claim 1, wherein at least a portion of the first semiconductor regions sandwich the trench gates via the gate-insulating film.

3. A semiconductor device according to claim 2, wherein the first semiconductor regions are formed along

the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-like configuration.

4. A semiconductor device according to claim 1, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-like configuration.

5. A semiconductor device according to claim 1, further comprising a wiring member connected to at least one of the plurality of trench gates.

6. A semiconductor device according to claim 2, further comprising a wiring member connected to at least one of the plurality of trench gates.

7. A semiconductor device according to claim 3, further comprising a wiring member connected to at least one of the plurality of trench gates.

8. A semiconductor device according to claim 4, further comprising a wiring member connected to at least one of the plurality of trench gates.

9. A semiconductor device according to claim 1,

further comprising a wiring member connected to the body region and to the second semiconductor region.

10. A semiconductor device according to claim 2, further comprising a wiring member connected to the body region and to the second semiconductor region.

11. A semiconductor device according to claim 3, further comprising a wiring member connected to the body region and to the second semiconductor region.

12. A semiconductor device according to claim 4, further comprising a wiring member connected to the body region and to the second semiconductor region.

13. A process for producing a semiconductor device comprising:

forming a body region of a first conductivity type in a semiconductor substrate;

forming a plurality of trench gates extending through the body region;

forming a plurality of first semiconductor regions of a second conductivity type that is different from the first conductivity type, the first semiconductor regions having a first depth as measured from a surface of the body region and sandwiching the trench gates via gate-insulating films;

forming a plurality of second semiconductor regions

of the second conductivity type having a second depth as measured from the surface of the body region that is less than the first depth; and

connecting the plurality of first semiconductor regions spaced apart from one another by the second semiconductor regions.

14. A process according to claim 13, wherein at least a portion of the first semiconductor regions sandwich the trench gates via the gate-insulating film.

15. A process according to claim 14, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-like configuration.

16. A process according to claim 13, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-like configuration.

17. A process according to claim 13, further comprising:

forming a wiring member connected to at least one of the plurality of trench gates.

18. A process according to claim 13, further comprising:

forming a wiring member connected to the body region and to the second semiconductor region.

ABSTRACT OF THE DISCLOSURE

A power semiconductor device having a low on-resistance and a high breakdown ruggedness is disclosed. Trench regions formed so as to contact trench gates via gate-insulating films are connected by emitter regions so as to form a ladder-like configuration. The emitter regions are formed at a less depth than the trench regions. Therefore, the resistance in portions of the body that are near the interfaces with the emitter regions is reduced, and the operation of parasitic transistors formed by the emitter regions, the body, and an epitaxial layer is substantially prevented. As a result, the on-resistance is varied, and the avalanche ruggedness and the latch-up ruggedness are improved.

FIG. 1

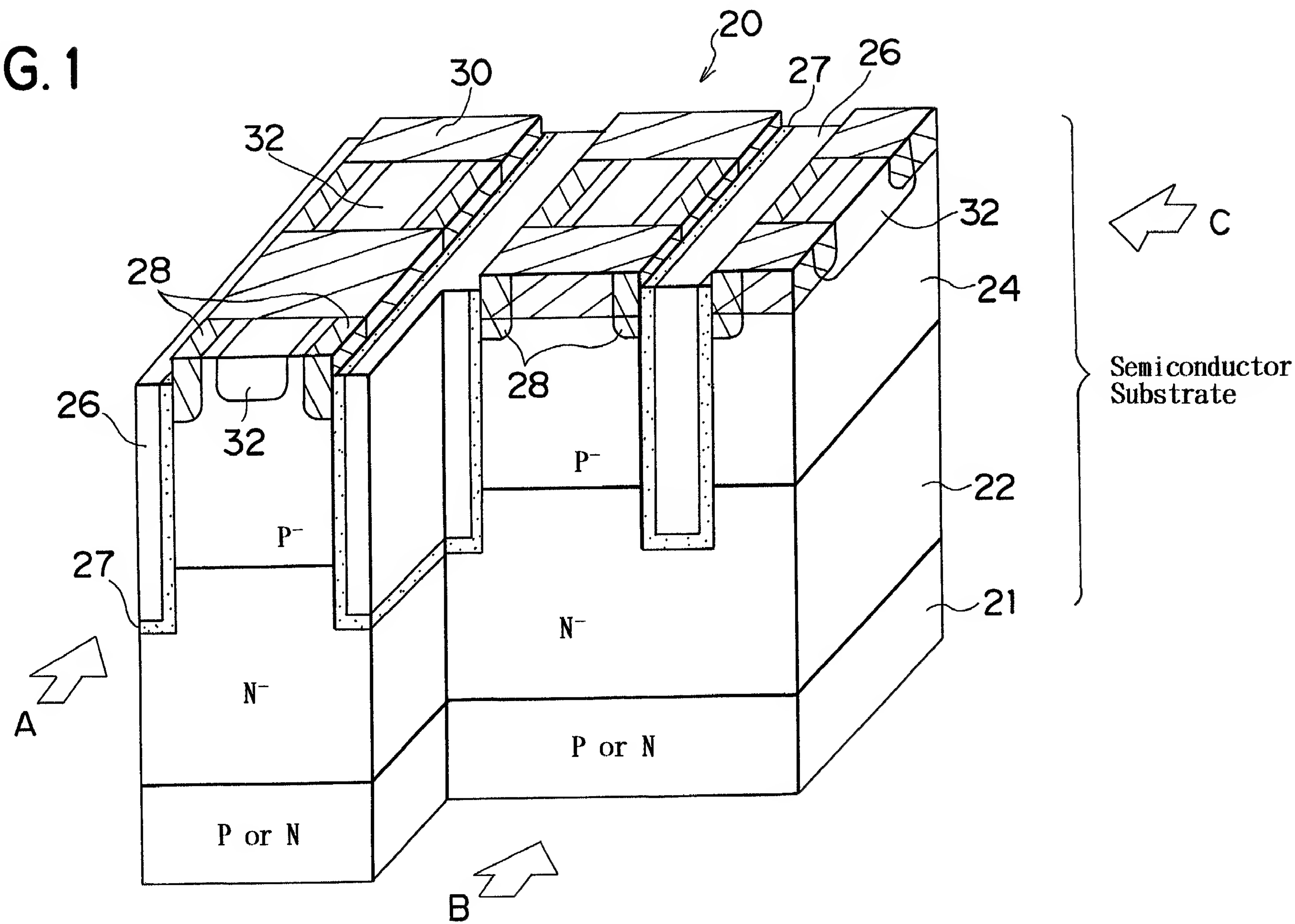

20
30
32
27
26
32
C
28
24
28
Semiconductor
Substrate
26
32
P⁻
22
P⁻
27
21
N⁻
N⁻
A
P or N
P or N
B

FIG. 2

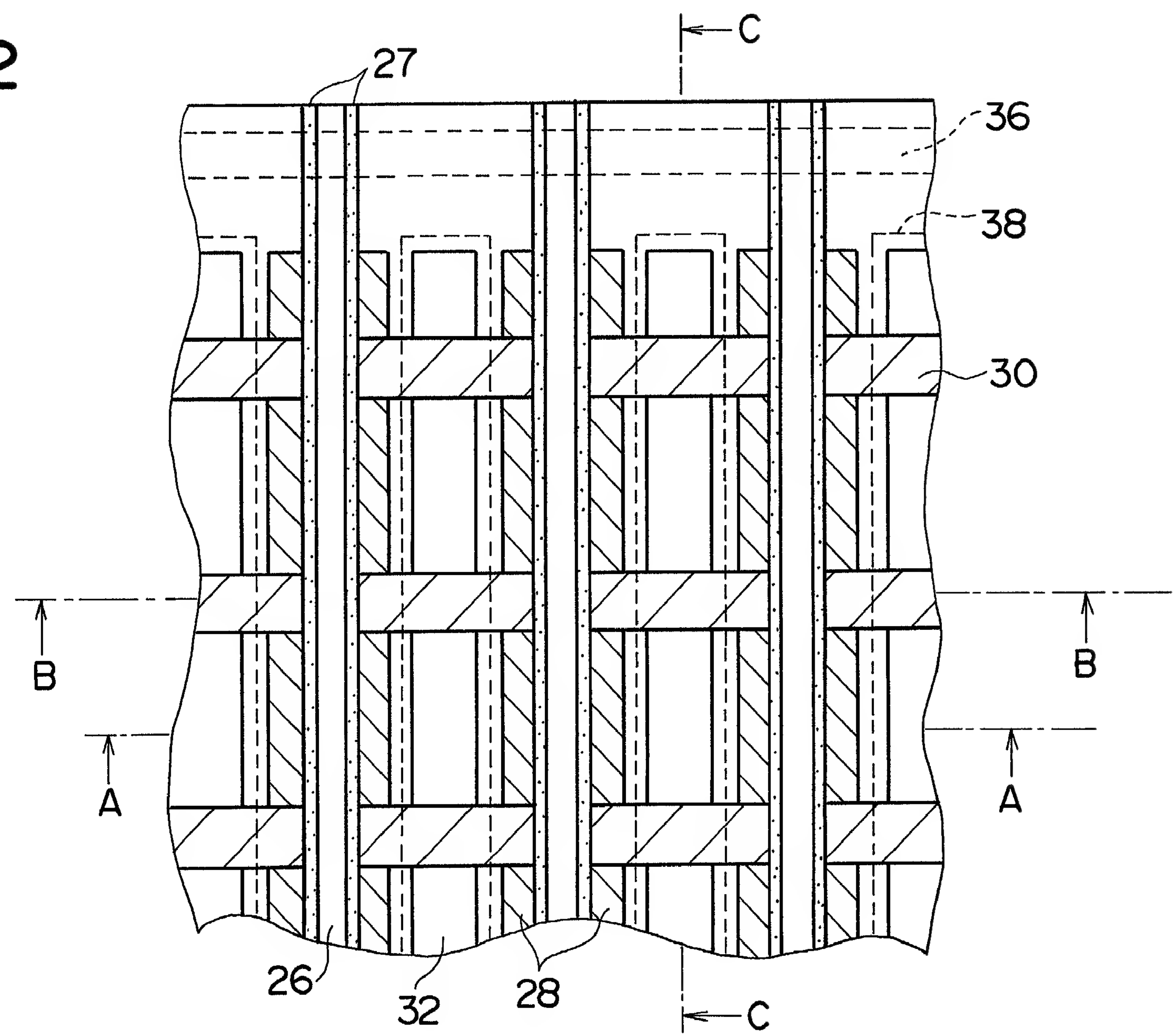


FIG. 3

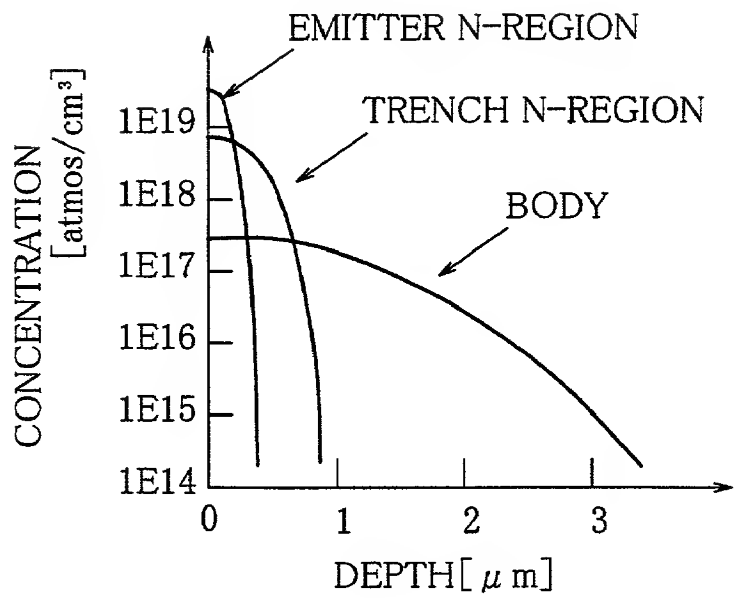


FIG. 4A

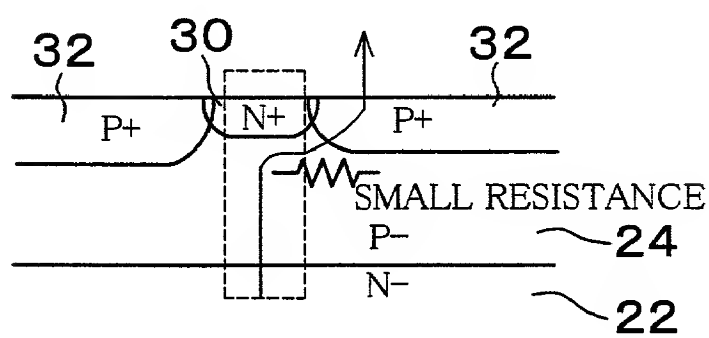
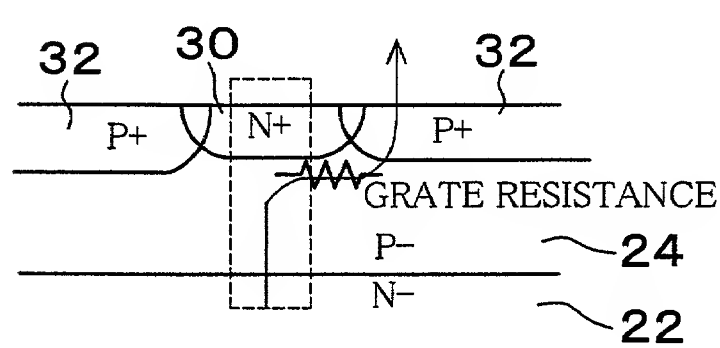


FIG. 4B



FOR UTILITY/DESIGN
CIP/PCT NATIONAL/PLANT
ORIGINAL/SUBSTITUTE/SUPPLEMENTAL
DECLARATIONS

RULE 63 (37 C.F.R. 1.63)
DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PM & S
FORM

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the INVENTION ENTITLED POWER SEMICONDUCTOR DEVICE AND PRODUCTION METHOD FOR THE SAME

the specification of which (CHECK applicable BOX(ES))

X BOX(ES)
→ A. ☒ is attached hereto.
→ B. ☐ was filed on ______ as U.S. Application No. ___/___
→ C. ☐ was filed as PCT International Application No. PCT/ ___/___ on ______

and (if applicable to U.S. or PCT application) was amended on ______

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F.R. 1.56. I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International Application which designated at least one other country than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International Application, filed by me or my assignee disclosing the subject matter claimed in this application and having a filing date (1) before that of the application on which priority is claimed, or (2) if no priority claimed, before the filing date of this application:

PRIOR FOREIGN APPLICATION(S) Number	Country	Day/MONTH/Year Filed	Date first Laid-open or Published	Date Patented or Granted	Priority Claimed Yes	No
HEI 11-262861	Japan	17/9/1999			X	

I hereby claim domestic priority benefit under 35 U.S.C. 119(e) or 120 and 365(c) of the indicated United States applications listed below and PCT international applications listed above or below and, if this is a continuation-in-part (CIP) application, insofar as the subject matter disclosed and claimed in this application is in addition to that disclosed in such prior applications, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F.R. 1.56 which became available between the filing date of each such prior application and the national or PCT international filing date of this application:

PRIOR U.S. PROVISIONAL, NONPROVISIONAL AND/OR PCT APPLICATION(S) Application No. (series code/serial no.)	Day/MONTH/Year Filed	Status pending, abandoned, patented	Priority Claimed Yes	No

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

And I hereby appoint Pillsbury Madison & Sutro LLP, Intellectual Property Group, 1100 New York Avenue, N.W., Ninth Floor, East Tower, Washington, D.C. 20005-3918, telephone number (202) 861-3000 (to whom all communications are to be directed), and the below-named persons (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent, and I hereby authorize them to delete names/numbers below of persons no longer with their firm and to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct the above Firm and/or a below attorney in writing to the contrary.

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(2) INVENTOR'S SIGNATURE: Date:

	First	Middle Initial	Family Name

	City	State/Foreign Country	Country of Citizenship
Residence			

Post Office Address (include Zip Code):

(FOR ADDITIONAL INVENTORS, check box ☐ to attach PAT 116-2 same information for each re signature, name, date, citizenship, residence and address.)